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Appl. No. 09/521,641 Supp. Amdt. dated August 7, 2006 Reply to Office Communication of July 19, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

- Claim 1 (previously presented): A method of performing additive synthesis of digital audio signals in a recursive digital oscillator, comprising:
 - receiving digital audio signal frames wherein each digital audio signal frame includes a set of frequency, amplitude, and phase components represented as coefficients of variables in a mathematical expression, each digital audio signal frame thereby including a frequency coefficient representation;
 - forming converted frequency coefficients by Re-Mapping of bits of said frequency coefficient representation to bias audio reproduction accuracy toward low frequency signals
 - wherein said digital oscillator is an oscillator as in claim 16 and wherein said Re-Mapping biases the generating frequency of said oscillator as in claim 17; and
- performing additive synthesis with said converted frequency coefficients.
- 1 Claim 2 (previously presented): The method of claim 1
- 2 further comprising the step of defining said frequency
- 3 coefficient representation with an exponent characterizing a
- 4 floating-point range extension.
- Claim 3 (previously presented): The method of claim 2
- 2 wherein said defining step includes the step of specifying

- Appl. No. 09/521,641 Supp. Amdt. dated August 7, 2006 Reply to Office Communication of July 19, 2006
- 3 said exponent to correspond to a right shift amount
- 4 necessary to correct for precision limitations introduced by
- 5 limiting Re-Mapping coefficients to 16 bits.
- 1 Claim 4 (previously presented): The method of claim 3
- 2 wherein said receiving, forming, and performing steps are
- 3 implemented utilizing a 16-bit fixed point processor.
- 1 Claim 5 (previously presented): The method of claim 1
- wherein said receiving, forming and performing steps are
- 3 implemented utilizing a digital signal processor.
- 1 Claim 6 (previously presented): The method of claim 1
- wherein said receiving, forming, and performing steps are
- 3 implemented utilizing a field programmable gate array.
- 1 Claim 7 (previously presented): The method of claim 1
- wherein said receiving, forming, and performing steps are
- 3 implemented utilizing a Very Long Instruction Word
- 4 processor.
- 1 Claim 8 (previously presented): The method of claim 1
- 2 wherein said receiving, forming, and performing steps are
- 3 implemented utilizing a Reduced Instruction Set Computer.
- 1 Claim 9 (previously presented): The method of claim 1
- wherein said receiving, forming, and performing steps are
- 3 implemented utilizing a Residue Number System processor.
- 1 Claim 10 (previously presented): A computer readable memory
- 2 to direct a processor to function in a specified manner,
- 3 comprising:

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Appl. No. 09/521,641
Supp. Amdt. dated August 7, 2006
Reply to Office Communication of July 19, 2006
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- a first set of executable instructions to receive digital audio signal frames wherein each digital audio signal frame has a set of specified frequency values expressed as a bit sequence;
- a second set of executable instructions to Re-Map said
 bit sequence to represent lower frequencies with more
 significant bits and higher frequencies with less
 significant bits; and
- a third set of executable instructions to facilitate
 additive synthesis of said digital audio signal frames in a
 reduced-precision recursive digital oscillator
 wherein said digital oscillator is an oscillator as in
 claim 16 and wherein said Re-Mapping biases the generating
 frequency of said oscillator as in claim 17.
- Claim 11 (previously presented): The computer readable
 memory of claim 10 wherein said first set of executable
 instructions include instructions to identify a frequency
- Claim 12 (previously presented): The computer readable
 memory of claim 11 further comprising a fourth set of
 executable instructions to define said frequency coefficient
 representation with an exponent characterizing a

coefficient representation of said specified frequency.

- 5 floating-point range extension.
- Claim 13 (previously presented): The computer readable
 memory of claim 12 wherein said fourth set of executable
 instructions include instructions to specify said exponent
 to correspond to a right shift amount necessary to correct
 for precision limitations introduced by a reduced precision
 processor.

Page 5 of 7

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Appl. No. 09/521,641
Supp. Amdt. dated August 7, 2006
Reply to Office Communication of July 19, 2006
Claims 14-15 (canceled)
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Claim 16 (previously presented): A recursive digital oscillator generating frequency f lying in the range from zero to one-half of a sampling frequency f_s comprising:

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recursion coefficients x_n given by

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$$x_{n} = 2x_{n-1} - \varepsilon x_{n-1} - x_{n-2}$$

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9 wherein $\epsilon = 2 - 2 \cos(\omega)$ and

wherein $\omega = 2\pi f/f_s$.

- 1 Claim 17 (previously presented): An oscillator as in
- claim 16 wherein ε is represented by an unsigned mantissa,
- 3 m, combined with an unsigned exponent, e, biased so that the
- 4 actual represented value is

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$$\varepsilon = 2^{2-e} m.$$

- 1 Claim 18 (previously presented): An oscillator as in
- 2 claim 17 wherein said mantissa m is 16 bits.